(2) Please rewrite Claim 21 as follows:

21. (Amended) A semiconductor device, comprising:

a first metal feature located over a semiconductor surface and having a first interlevel dielectric layer located thereover and a second interlevel dielectric layer located over the first interlevel dielectric layer, the second interlevel dielectric layer having a second metal feature located in a surface thereof; and

an unsegmented via located through the first and second interlevel dielectric layers, the via extending between and connecting the first metal feature and the second metal feature, the via being void of a landing pad between the first and second interlevel dielectric layers.

## REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicant originally submitted Claims 1-28 in the present application. Pursuant to a restriction requirement, Claims 1-20 were previously withdrawn without traverse. The Applicant presently amends Claim 21 and cancels Claims 1-20 without prejudice or disclaimer. Accordingly, Claims 21-28 are currently pending in the application.

Additionally, support for the amendments to Claim 21 may be found in the originally filed application. For instance, a via extending continuously between first and second metal features can be found in FIGURE 3 and supporting text on page 12, line 17 through page 13, line 22, as well as in FIGURE 1 and supporting text on page 16, lines 8-10. As seen from FIGURE 3, this via, which extends through both dielectric layers, is unsegmented (*i.e.*, is continuous) in that it contains no

metal interfaces as do the vias disclosed in the cited references. Moreover, in view of the teachings of the application as a whole, the via would be unsegmented, or continuous, given the way in which it was made.

In addition, one having ordinary skill in the pertinent art understands that the first and second dielectric layers disclosed in the specification and the FIGUREs of the present application are, in fact, interlevel dielectric layers conventionally employed in interconnect structures, in contrast to mere etch stop layers, as the Examiner has asserted. Accordingly, the recitation of first and second interlevel dielectric layers in Claim 21 is supported in the specification by the references to interlevel structures. Therefore, the amendments communicated herein do not add new subject matter to the originally filed application.

## I. Rejection of Claims 21-24 and 26 under 35 U.S.C. §102

The Examiner has rejected Claims 21-24 and 26 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,020,255 to Tsai, *et al.* ("Tsai"). However, Tsai fails to disclose an unsegmented via located through first and second interlevel dielectric layers, as recited in Claim 21 of the present application. In contrast, Tsai merely discloses a via 115 extending between a single dielectric layer 120 and an etch stop layer 130. (Column 4, line 66 - column 5, line 45; Fig. 3e). One of ordinary skill in the art understands that interlevel dielectric layers and etch stop layers are not the same and serve two entirely different purposes within a semiconductor device.

Because Tsai fails to disclose an unsegmented via located through first and second interlevel dielectric layers, Tsai is not an anticipating reference for Claim 21. Because Claims 22-24 and 26 are dependent upon Claim 21, Tsai also cannot be an anticipating reference for Claims 22-24 and

26. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 21-24 and 26.

## II. Rejection of Claims 21, 24, 25, 27 and 28 under 35 U.S.C. §102

The Examiner has rejected Claims 21, 24, 25, 27 and 28 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,654,589 to Huang, *et al.* ("Huang"). However, Huang fails to disclose an unsegmented via extending between and connecting first and second metal features and being void of a landing pad between first and second interlevel dielectric layers, as recited in Claim 21 of the present application. In contrast, Huang discloses a series of Ti/TiN stack interconnect structures 32 (shown in Fig. 1d) that are produced from an etched layer of Ti 28 and an etched layer of TiN 30. These Ti/TiN stack interconnect structures 32 serve as local interconnects and contact landing pads. (Column 5, line 54 - column 6, line 19). Therefore, Huang discloses interconnect structures specifically including landing pads, which is contrary to the presently claimed invention.

Because Huang fails to disclose an unsegmented via extending between and connecting first and second metal features and being void of a landing pad between first and second interlevel dielectric layers, Huang is not an anticipating reference for Claim 21. Because Claims 24, 25, 27 and 28 are dependent upon Claim 21, Huang also cannot be an anticipating reference for Claims 24, 25, 27 and 28. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 21, 24, 25, 27 and 28.

## III. Rejection of Claims 21-24 and 26-28 under 35 U.S.C. §102

The Examiner has rejected Claims 21-24 and 26-28 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,834,8455 to Stolmeijer, *et al.* ("Stolmeijer"). However, Stolmeijer fails to disclose an unsegmented via located through first and second interlevel dielectric layers and extending between and connecting first and second metal features, as recited in Claim 21 of the present application. In contrast, Stolmeijer merely discloses forming multiple patterned metal layers 36a-e on top of one another (column 4, line 40 - column 5, line 32), wherein each patterned metal layer 36 is the same thickness as the surrounding dielectric 38, 40 (column 5, lines 33-41). Therefore, the interlevel connections disclosed in Stolmeijer comprise several layers of metal having metal interfaces at each individual layer, in contrast to an unsegmented via extending between and connecting metal features inherently located on different layers of the structure.

Because Stolmeijer fails to disclose an unsegmented via located through first and second interlevel dielectric layers and extending between and connecting first and second metal features, Stolmeijer is not an anticipating reference for Claim 21. Because Claims 22-24 and 26-28 are dependent upon Claim 21, Stolmeijer also cannot be an anticipating reference for Claims 22-24 and 26-28. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 21-24 and 26-28.

## IV. Rejection of Claim 25 under 35 U.S.C. §103

The Examiner has rejected Claim 25 under 35 U.S.C. §103(a) as being unpatentable over Stolmeijer. However, Stolmeijer fails to teach or suggest an unsegmented via located through first and second interlevel dielectric layers and extending between and connecting first and second metal features, as recited in Claim 21 of the present application. As discussed above, Stolmeijer merely

teaches a segmented stack of patterned metal layers 36. In addition, the shortcomings of Stolmeijer are not corrected by the Examiner's assertion that it would have been obvious to one of ordinary skill in the art to modify the device of Stolmeijer to include transistors to provide different desired functions. (Examiner's Action, page 6). Specifically, such a modification also fails to teach or suggest an unsegmented via located through first and second interlevel dielectric layers and extending between and connecting first and second metal features. Moreover, one skilled in the art would not be motivated to modify these teachings because Stolmeijer specifically teaches a via formed through only one interlevel dielectric at a time. Given the complexities associated with modifying any single step in an integrated circuit design, there is no suggestion, absent the use of hindsight, to arrive at the claimed invention.

Therefore, Stolmeijer fails to support a *prima facie* case of obviousness with respect to Claim 21. Because Claim 25 is dependent upon Claim 21, Stolmeijer also fails to support a *prima facie* case of obviousness with respect to Claim 25. Accordingly, the Applicant requests the Examiner to withdraw the §103 rejection with respect to Claim 25.

## V. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 21-28.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

(1) Please cancel Claims 1-20 without prejudice or disclaimer.

(2) Please rewrite Claim 21 as follows:

21. (Amended) A semiconductor device, comprising:

a first metal feature located over a semiconductor surface and having a first interlevel dielectric layer located thereover and a second interlevel dielectric layer located over the first interlevel dielectric layer, the second interlevel dielectric layer having a second metal feature located in a surface thereof; and

[a] an unsegmented via located through the first and second interlevel dielectric layers, the via extending between and connecting the first metal feature and the second metal feature, the via being void of a landing pad between the first and second interlevel dielectric layers.